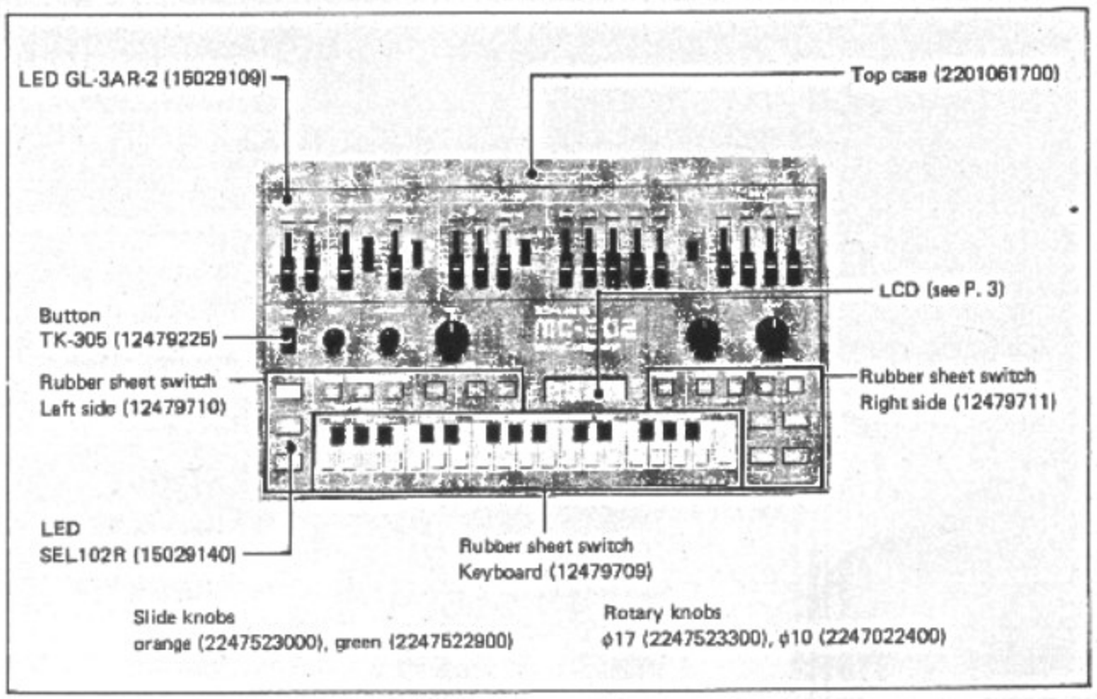
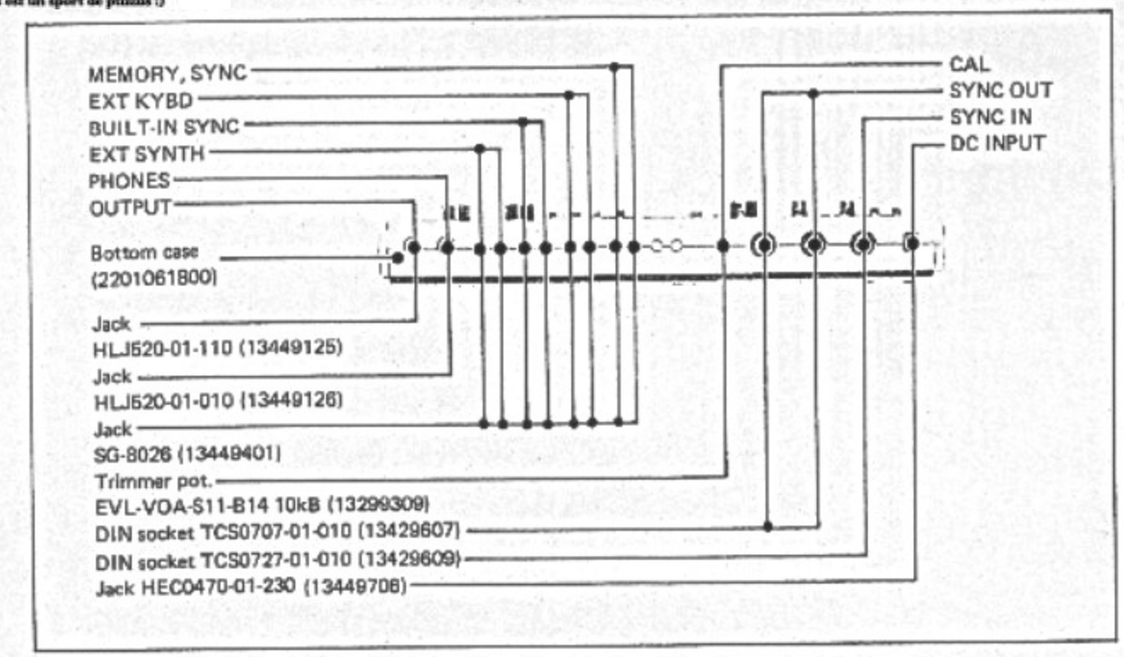
MC-202 SERVICE NOTES *First Edition*

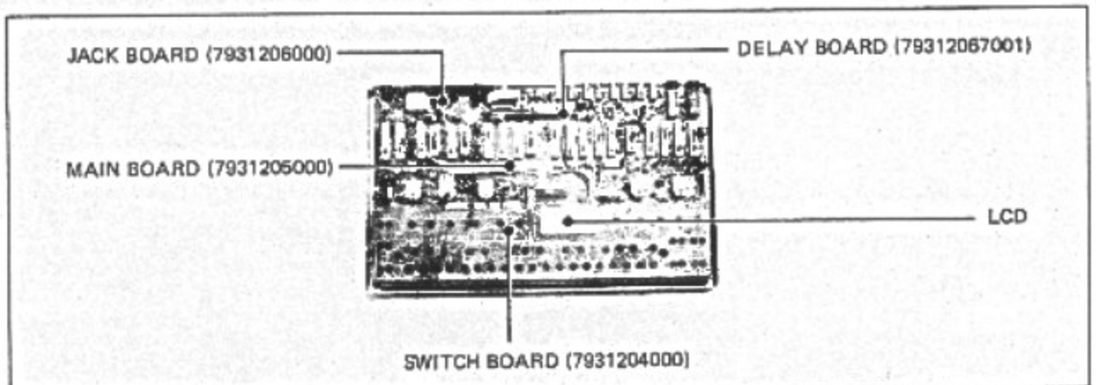
SPECIFICATIONS

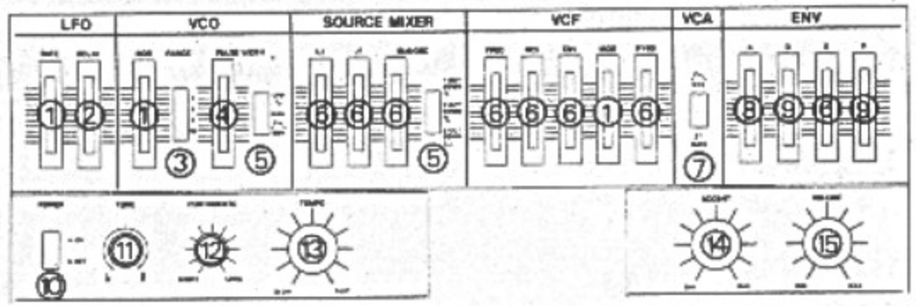
- Memory Capacity: Approx. 2600 steps
- Output: External CV Output .... 416.5mV to 5V, 44 steps (Built-in Keyboard)
  .... 0V to 5V, 49 steps (83.3mV/step) (External Keyboard)
  External Gate Output .... ON: +12V
  .... OFF: 0V
- Input (Keyboard Input): CV IN .... 0V to 5V
  GATE IN .... Over +3V
  Calibration Trimmer .... ± 50mV max.
- Tempo Range: ♩ = 40 to 300
- Keyboard: 32 Key, F scale
- VCO: Range .... 16', 8', 4'
  Pulse Width Modulation .... 0 to 50%
  Tune .... ± 100 cents
- VCF: Cutoff Frequency .... 10Hz to 20kHz
  Keyboard Follows .... 0 to 100%
- ENV: Attack Time .... 2ms to 1.5s
  Decay Time .... 2ms to 5s
  Sustain Level .... 0 to 100%
  Release Time .... 1ms to 5s
- LFO: Rate .... 0.1Hz to 30Hz
  Delay Time .... 0 to 1s
- PORTAMENTO: Time .... 0 to 2s
- Connection Jacks: Output .... 0dBm (max.)
  Headphones .... Stereo, 8Ω to 150Ω
- Power Source: 9V, battery or AC adaptor
- Power Consumption: 800mW
- Dimensions: 343(W) x 55(H) x 204(D) mm
  13-1/2(W) x 2-3/16(H) x 8(D) in
- Weight: 1.35kg (3 lb.) (including batteries)

TOP VIEW









1	Pot.	S2018P405-100kA	(13339328)	9	Pot.	S2018P405-1MA	(13339332)
2	Pot.	S2018P405-500kB	(13339333)	10	Switch	SUT-111	(13129324)
3	Switch	SQPR24-12P	(13159503)	11	Pot.	EVH5XAP20-10kB	(13219277)
4	Pot.	S2018P405-10kB	(13339330)	12	Pot.	EWK77AP20-1MA	(13219779)
5	Switch	SSB-02335	(13159304)	13	Pot.	EVH5XAP20-1MC	(13219279)
6	Pot.	S2018P405-100kB	(13339329)	14	Pot.	EVH5XAP20-100kB	(13219280)
7	Switch	SSB-02242	(13159103)	15	Pot.	EVH5XAP20-100kA	(13219278)
8	Pot.	S2018P405-250kA	(13339331)				

CASE

2201061700	Top Case	
2201061800	Bottom Case	
2202064000	Battery Cover	
2202064100	Battery Holder	

PCB

7931205000	Main Board	(pcb 2291055500)
7931204000	Switch Board	(pcb 2291055600)
7931206000	Jack Board	(pcb 2291056600)
7931207000	Delay Board SN up to 303900	(pcb 2291058600)
7931207001	Delay Board SN 304000 and up	(pcb 2291077200)

RUBBER SHEET SWITCH

12479709	Keyboard	
12479710	Left Side	START, STOP/CONT, SHIFT etc.
12479711	Right Side	TAP, BAR, ENTER etc.

SWITCH

13129324	SUT-111 (push)	POWER SW
13159304	SSB-02335 (slide)	VCO(PWM)
13159103	SSB-02242 (slide)	VCA(ENV/GATE)
13159503	SQPR24-12P (slide)	VCO(RANGE)

KNOB

2247523000	Slide Pot(orange)	ALL EXCEPT SOURCE MIXER
2247522900	Slide Pot(green)	SOURCE MIXER
2247523300	Rotary Pot(orange)	TEMPO, ACCENT, VOLUME
2247022400	Rotary Pot(orange)	TUNE, PORTAMENTO

BUTTON

12479225	TK-305(black)	power switch

JACK

13449125	HLJ520-01-110 mono, ϕ6.5	OUTPUT
13449126	HLJ520-01-010 stereo, ϕ6.5	PHONES
13449401	SG-8026 3.6ϕ	CV, GATE IN/OUT etc.
13449706	HEC0470-01-230 DC input	DC IN
13429607	TCS0707-01-010	DIN OUT
13429609	TCS0727-01-010 with Switch	DIN IN

IC

15179139	µPD78C06G-024-11	CMOS CPU
15159101H0	HD14001BP	Quad 2-input NOR gate
15159104H0	HD14011BP	Quad 2-input NAND gate
15159105H0	HD14013BP	Dual D flip-flop
15159128H0	HD14050BP	Hex Buffer
15159114H0	HD14052BP	Dual 4ch Multiplexer
15159115H0	HD14066BP	Quad Analog Switch
15159306H0	HD14503BP	Hex 3-state Buffer
15159301H0	HD14520BP	Dual Binary Up Counter
15159303H0	HD14584BP	Hex Schmitt Trigger
15159110T0	TC4030BP	Quad 2-input Exclusive NOR
15159312H0	HD14519BP	Quadruple 2ch Data Selector
15159137H0	HD14015BP	Dual Shift Resistor
15179313	M5K4164 P-20	64K D-RAM
15189115	TL022CP	Low-power OP-AMP
15189119	TL062CP	Low-power Bi-FET OP-AMP
15189118J0	NJM082DR	OP-AMP
15189136	M5218L	OP-AMP
15189138	AN6562	OP-AMP
15229802	BA662A	VCA
15229801	IR-3109	VCF
15229810	CEM3340	VCO
15169509	MN1252B	LCD Driver

TRANSISTOR

15119105	2SA733(P)
15119602	2SB647(C)
15129108	2SC945(P)
15129602	2SD667(C)
15129412	2SC1384(Q)
15139101	2SK30ATM-Y

DIODE

15019557	RD15EB3	
15019303	RD5.6JB2	
15019630	1SZ46A	
15019125	1SS-133	
15019208	1SR35-200	
15029109	GL3AR-2	(LED) LFO
15029140	SEL102R	(LED) START

POTENTIOMETER

(SLIDER)		
13339330	S2018P405-10K(B)	VCO(PWM)
13339328	S2018P405-100K(A)	LFO(RATE), VCO(MOD), VCF(MOD)
13339329	S2018P405-100K(B)	SOURCE MIXER, VCF(FREQ, RES, ENV, KYBD), ENV(S)
13339331	S2018P405-250K(A)	ENV(A)
13339333	S2018P405-500K(B)	LFO(DELAY)
13339332	S2018P405-1M(A)	ENV(D, R)
(ROTARY)		
13219277	EVH5XAP20-10K(B)	TUNE
13219278	EVH5XAP20-100K(A)	VOLUME
13219280	EVH5XAP20-100K(B)	ACCENT
13219279	EVH5XAP20-1M(C)	TEMPO
13219779	EWK77AP20-1M(A)	PORTAMENTO

TRIMMER

13299558	RVS0707V101-3-301 thermet(blue)	300
13299554	RVS0707V101-3-502	5K
13299562	RVG0707V101-10-503 thermet(black)	50K
13299141	RVF8P01-204 carbon	200K
13299142	RVF8P01-504	500K
13299136	RVF8P01-503	50K
13299309	EVL-VOA-S11-B14 10K (CAL)	

RESISTOR (Metal Film)

13769154T0	1.69K	MR25 1%	100ppm
13769167T0	5.6K	MR25 1%	100ppm
13769256T0	28K	MR25 1%	100ppm
13769187T0	39K	MR25 1%	100ppm
13769197T0	100K	MR25 1%	100ppm
13769204T0	200K	MR25 1%	100ppm
13769207T0	270K	MR25 1%	100ppm
13769215T0	560K	MR25 1%	100ppm
13769257T0	1.5M	MR25 1%	100ppm

RESISTOR ARRAY

13919121	RNSA09P473	47K x 8

OTHERS

2345012500	Terminal Board Battery	+ side
2345012600	Terminal Spring Battery	- side
15029408	EDD063M04B3 LCD Display Panel	
2219031400	LCD Display Panel Holder	
2343051300	Rubber strip	
2345090500	Rubber strip (conductive)	
12449513	LC-14	DC/DC CONV.
12389710	FCR-5M	Ceramic Resonator
12389711	PKM24-4A0	Piezo Alarm
15229908	SDT-1000	Thermister

IC7 M5K4164 P-20 is a 65,536 words by 1 bit Dynamic N-MOS RAM(D-RAM). In the MC-202 circuitry the D-RAM is configured as an 8,192 words by 8 bits memory and is operated in a page mode.

At the beginning of a memory cycle $\overline{REF}$ is removed from IC7 to defeat the refreshing cycle. A row address at A0-A7 of IC7 is strobed into chip with $\overline{RAS}$ when IC3c, d flip-flop is set by delayed CPU $\overline{WR}$, selecting one of the 256 rows.

On the next CPU $\overline{WR}$, another flip-flop IC2a, b reverses pins 3 and 4.

Output at pin 4 is applied to two places.

1) Pin 8 of the CPU as a $\overline{WAIT}$, telling the CPU to hold the processed data waiting until the $\overline{WAIT}$ goes high.

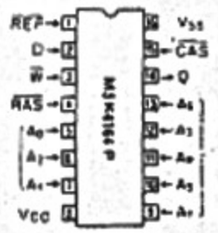
2) Pin 4 of IC5a through R33 as a CK, causing it to count CPU ϕ OUT and have respective outputs at Q0-Q3. A specific combination of Q1-Q3 defines higher order bits of a column address which has been left undifined by software.

Outputs from pin 3 of IC2a and pin 3(Q0) of IC5a cause IC3b to have $\overline{CAS}$ which enables IC7 to strobe column address into the chip.

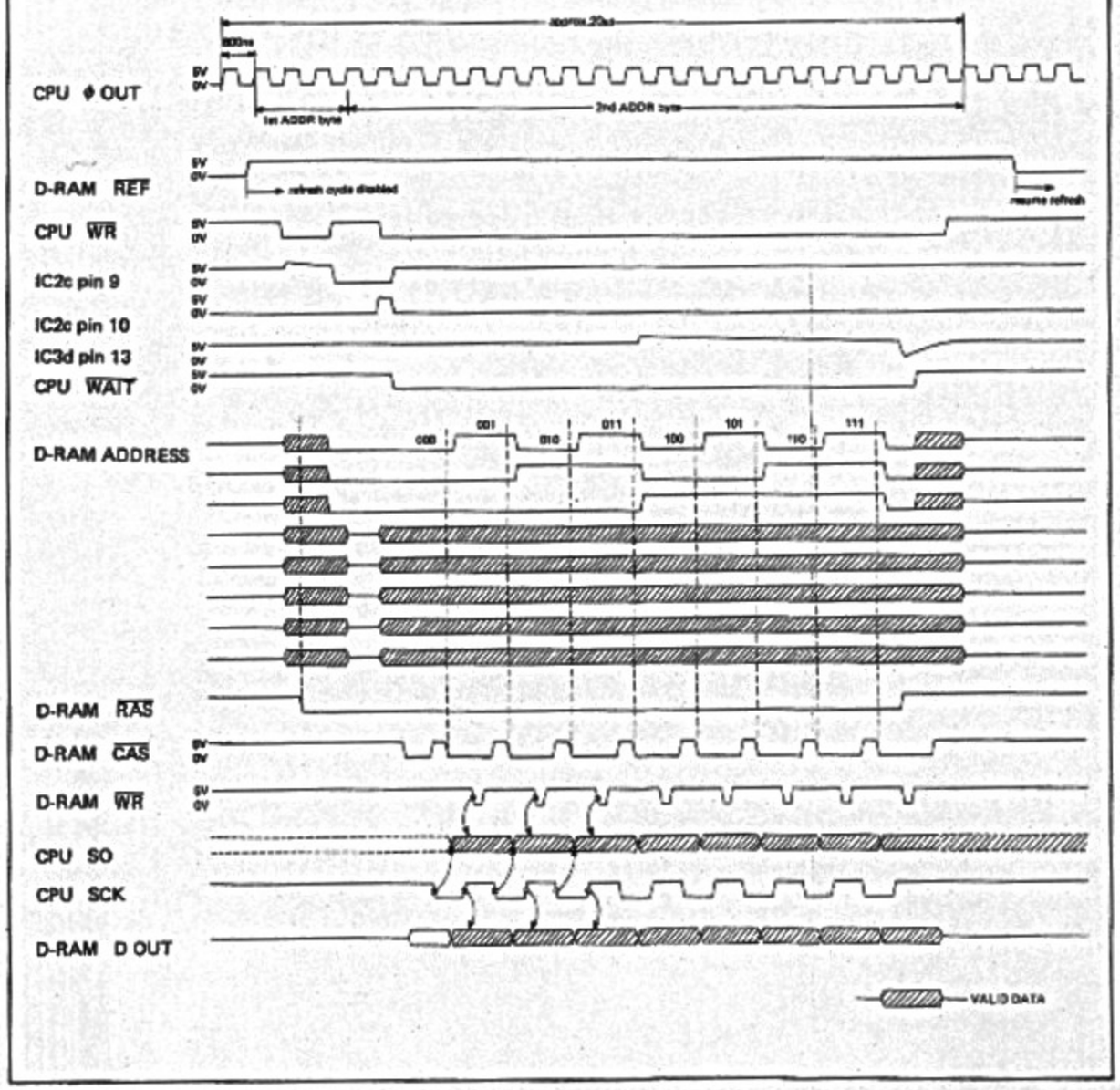
Q0 is also applied to two other places.

1) CPU as a $\overline{SCK}$ through IC4b, ticking serial data chain being transferred between the CPU and D-RAM IC7.

2) IC7 as RAM $\overline{WR}$ through IC2a and 4a when pin 13 of IC2d is low, allowing data to be stored into the chip.



MC-202 MEMORY CYCLE TIMING CHART



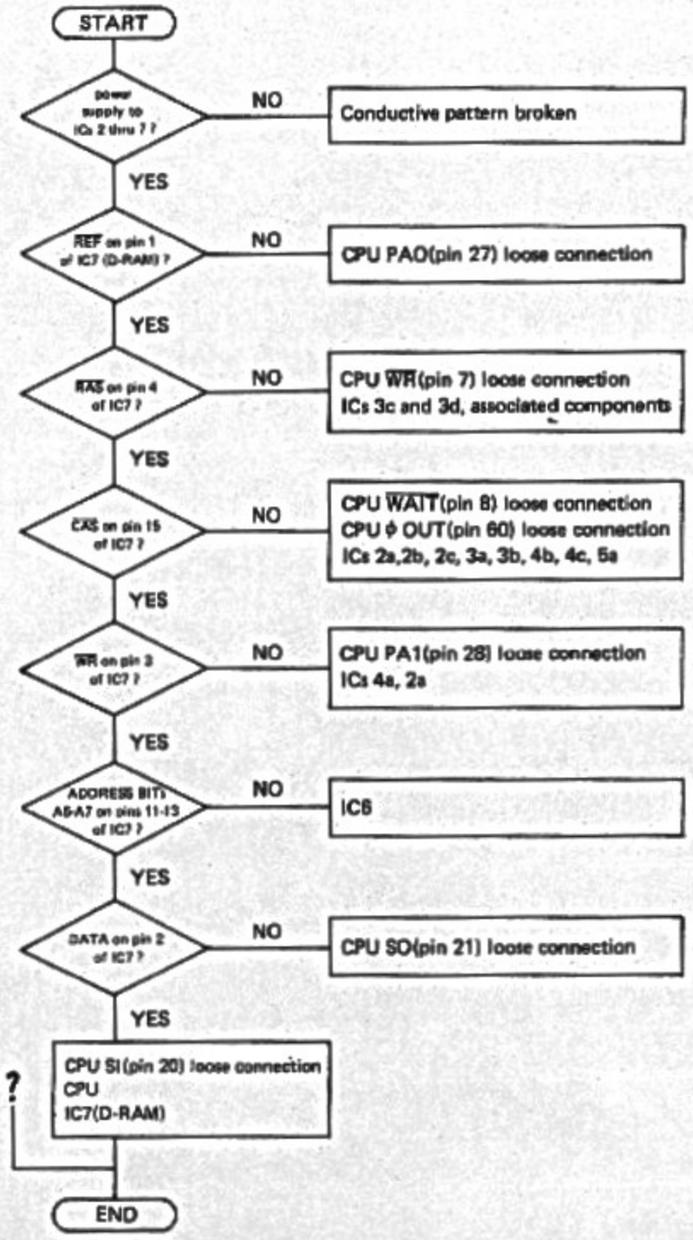
TROUBLESHOOTING MEMORY CIRCUITRY

The following chart will help in fault discovering of memory circuits. The MC-202 MEMORY CYCLE TIMING CHART should also be referred to for visual comprehension.

When the CPU is suspective, first check CPU pins for loose connection including cold joint, disturbed solder connection and poor adhesion. In doing so, use a small knife as a tool; insert the blade between CPU pin and conductive pattern to disclose unsoldered pin.

FAULT ISOLATION CHART

(Particular setup is unnecessary for checking – the MC-202 is set in the WRITE mode when the power is applied.)



CIRCUIT DESCRIPTIONS

The MC-202 hardware is divided into five basic sections as shown in the figure below.
The following description will mainly concentrate on digital aspects of the MC-202 circuitry.

CPU

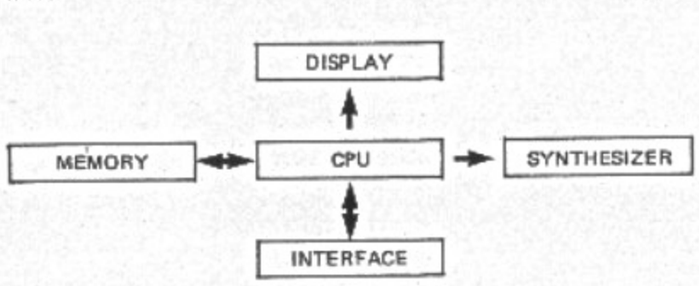
IC8 is an 8-bit microcomputer consisting of 8-bit ALU, ROM, RAM, Timer, Serial Interface and 46 I/O lines, all fabricated on a single chip. Some pin functions are directly denoted on the circuit diagram, respectively.

INT 0 (active high)

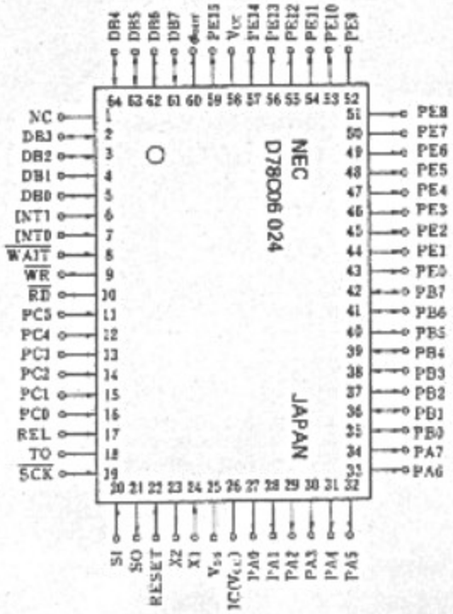
When the CPU senses a high at INT 0 pin, it begins fractions of Panel switch reading, CVs refresh and display data transfer in time sequence. The CPU repeats the cycle for the subsequent fractions at INT 0 rate. This interrupt signal has priority over INT 1.

INT 1 (active rising edge)

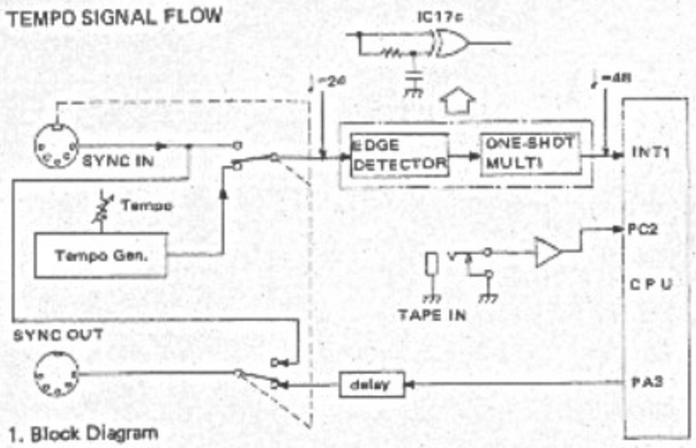
This signal is either Internal Tempo Clock or External one selected by IC16. The selected tempo clock triggers IC17c on every positive and negative edges to have doubled frequency at pin 10 of IC17c – 48 clocks/quarter.
The clocks are the time base for STEP TIME and GATE TIME in the PLAY mode.



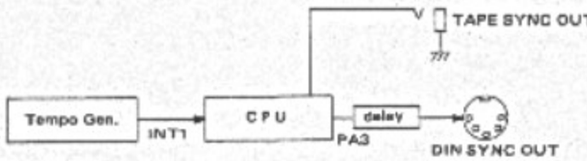
μPD78C06G
Pin configuration
(Top view)



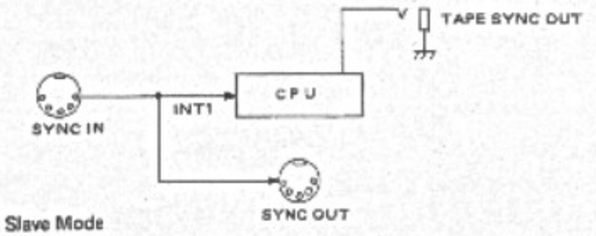
TEMPO SIGNAL FLOW



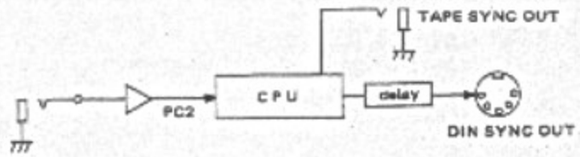
1. Block Diagram



2. Master Mode



3. Slave Mode



4. Tape Sync Mode

DELAYED SYNC OUTPUTS

For positive synchronization with an external equipment being engaged with the MC-202, the internally generated START/STOP, TEMPO and CONT signals are passed onto SYNC OUT DIN sockets through delay circuits.
The delay circuits will prevent the following problems from occuring at the external equipment.

- An odd sound after the end of the last measure.
- CONT is ignored.

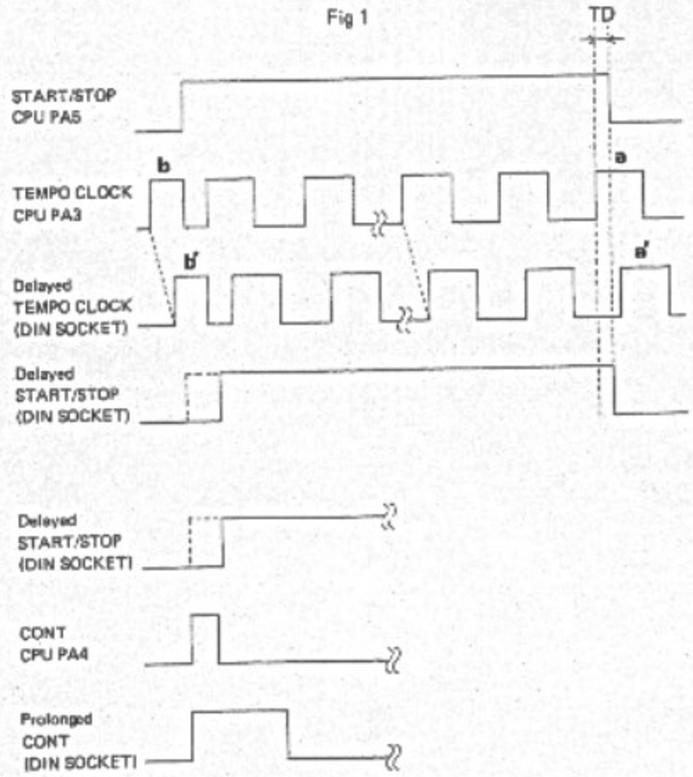
TEMPO CLOCK

When a measure has been completed, the CPU checks the D-RAM memory to know if there is a data to be taken for further process. It takes a time period of TD for the CPU to make the decision.
This TD allows the tempo clock **a** to reach the external device and to trigger its sound source, sounding an odd note.

The delay circuit IC30 inserted in SYNC OUT path eventually delays the entire tempo clocks so that clock **a'** goes high after TD has passed.

NOTE: Due to the characteristics of the Shift Register IC30, the delayed Tempo Clocks slightly jitter, having no ill effect on actual applications.

Fig 1



START/STOP

The delayed tempo clocks will bring an adverse effect upon START ON.
It is obvious from Fig. 1 that when the Tempo oscillator is reset by the rising edge of a START, unnecessary clock **b'** can trigger one of external sound sources because they have been enabled by the high START.
This **b'** will in turn bring a redundant clock at the end of the last measure, causing the same ill effect as **a** mentioned under TEMPO CLOCK.

Start Delay Circuit consisting of R501, D501 and C59 effectively delays the rising edge of the START signal behind **b'**, but does not affect on the transition of START to STOP.

CONTINUE

In Roland products, pressing CONTINUE button on their own panel generates a CONT signal and a concurrent START signal.
In accepting these signals as external control signals, any Roland product first senses START signal, then checks CONT for its presence. To keep pace with the delayed START, the falling edge of the CONT is sustained for a time enough for the external unit to detect it.

DISASSEMBLY

1. Remove 7 screws from the bottom and remove the lower case.
   Most of troubleshooting can be made with the foil sides of the PCBs exposed. The PCB layouts viewed from the foil side are provided on this manual just for this purpose.
   When need arises to expose the component sides:
2. Remove all knobs on the top panel.
   - small but useful hints -
   Rotary knob – by finger, with a rubber sheet wrapped around the knob face.
   Slide knob – with pliers. Insert a cloth between the jaws and the knob faces.
3. Remove the top case.
4. Peel the switch sheets off the top case and place them on the switch board.

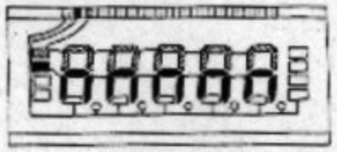
CAUTION

When separating Switch board from Main board, do not remove any screw on Switch board, instead extract PCB spacers from Main board by releasing the locks at the foil side of Main board.

REASSEMBLY

1. Place PCB assemblies into lower case.
2. Clean contact pads on Switch board with an alcohol.
3. Install top case.
   It is advisable to confirm all switch functions before mounting knobs.

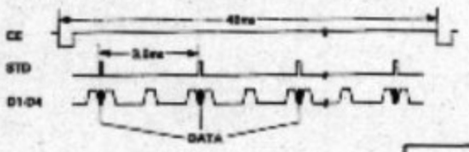
EDD063M04B3 is a field effect type Liquid Crystal Display. Each segment is composed of two electrodes placed on the opposite sides of the liquid crystal fluid. One electrode group is divided into three subgroups (Common) and the other into 16 (Segment) as shown in the figure below. They make up a 3 x 16 matrix.

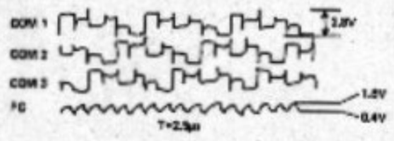


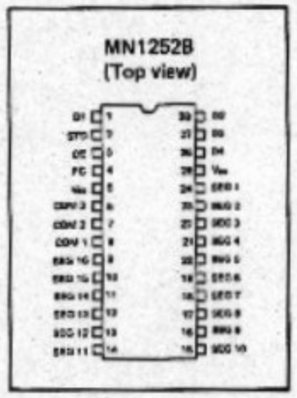
COMMON (3)

SEGMENT (16)

IC29 latches character codes (D1-D4) into buffers on STD pulse and drives LCD in dynamic method at the frame clock rate.

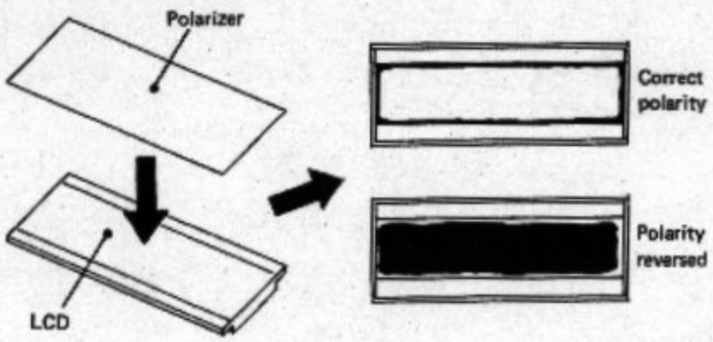




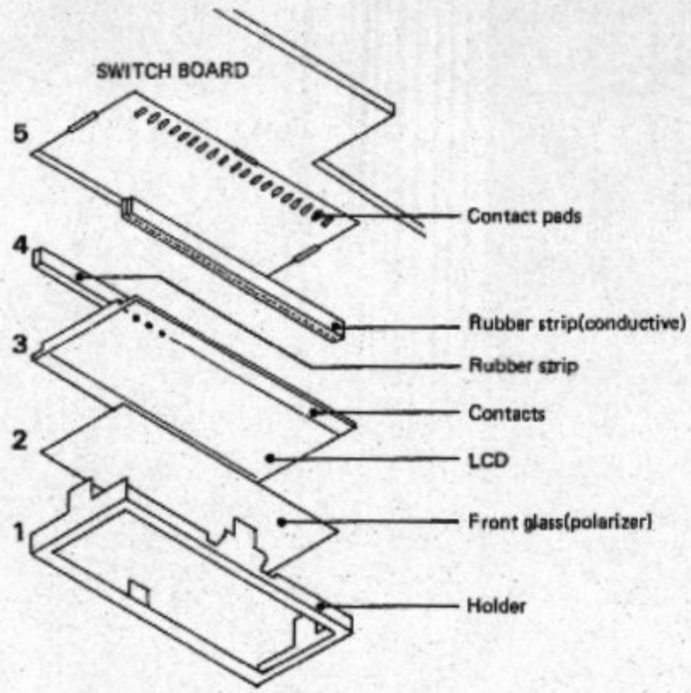


ASSEMBLING LCD UNIT

Assembling is better done by following the order numbered in the figure.



CAUTION:
Place the polarizer on the LCD with the front facing outside. Otherwise the readout is white characters on a dull black background.



ADJUSTMENT

1. INTERRUPT CLOCK

1-1. Connect oscilloscope to pin 12 of IC4f.
1-2. Adjust TM1 (INT) for 2ms/cycle.

2. TEMPO CLOCK

2-1. Connect the scope to pin 11 of IC5b.
2-2. Set TEMPO control (VR7) to FAST.
2-3. Adjust TM2 (TEMPO) for 8.33ms/cycle.

3. D/A REFERENCE VOLTAGE

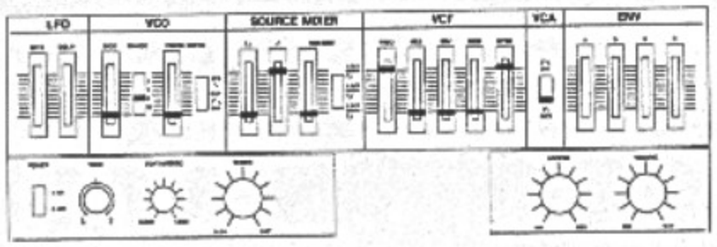
3-1. Connect digital voltmeter to pin 1 of IC11 (or IC12).
3-2. Adjust TM3 for +5.333V.

4. VCO

CAUTION

CAL on the Rear Panel
This is an adjustment to minimize pitch difference between EXT KYBD IN and the Internal KCV. If EXT IN jack is engaged without CAL readjusted, pitch drift will be heard in the beginning of every note. When adjusting, keep in mind that the CAL might have been set to tune the MC-202 to the user's EXT system.
FACTORY-ADJUSTMENT
CAL is set where no pitch difference is detected when 2,000V is applied from C3 key on an external keyboard.

The following calibration procedure is described using Lissajous method.
Connect the V IN of the scope to the MC-202 OUTPUT and H IN (EXT) to a standard tone generator (or tuner) referenced to 442Hz at A4.
Set the MC-202 as indicated.



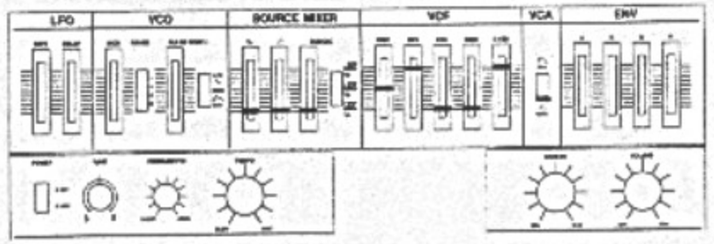
4-1. VCO Width
4-1-1. Set the generator for F note.
4-1-2. While holding 4F key, adjust VR3(TUNE) or TM5(TUNE) for still Lissajous.
4-1-3. Holding 2F key, adjust TM6 (VCO Width) for still Lissajous.
4-1-4. Repeat steps 4-1-2 and 3 until no further improvement can be made.

4-2. VCO Tune
4-2-1. Center VR3(TUNE).
4-2-2. Set the generator for 442Hz(A4).
4-2-3. Holding 3A, adjust TM5(TUNE) for still Lissajous.

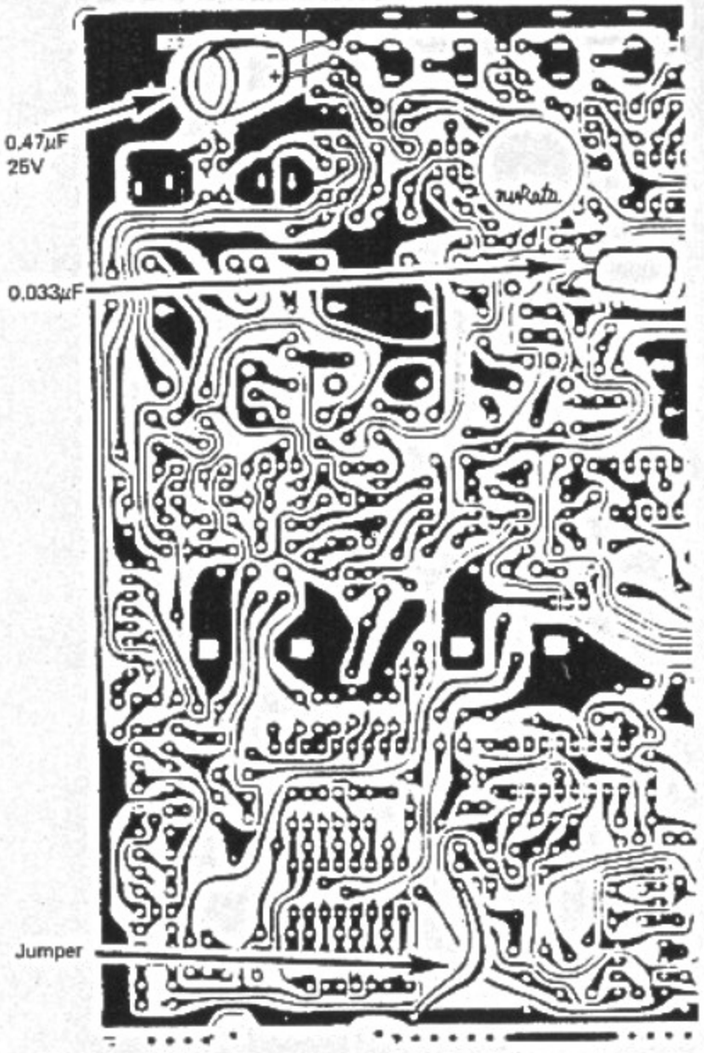
4-3. Pulse Width
4-3-1. Raise VR8(⊓) to the top.
4-3-2. Lower VR9(⌿) to the bottom.
4-3-3. Adjust TM4(PWM) for equal mark and space period.

5. VCF WIDTH

5-1. Set the scope H to INT.
5-2. Set the panel controls as indicated.



5-3. Holding 3A key, adjust VR11(FREQ) for approximately 1kHz.
5-4. Alternately playing 3F and 4F keys, adjust TM7(VCF WIDTH) until 4F waveform doubles 3F waveform in frequency.



CHANGE INFORMATION

The following modifications should be checked on a given unit for implementation and, if not found, be done to eliminate problems described below.

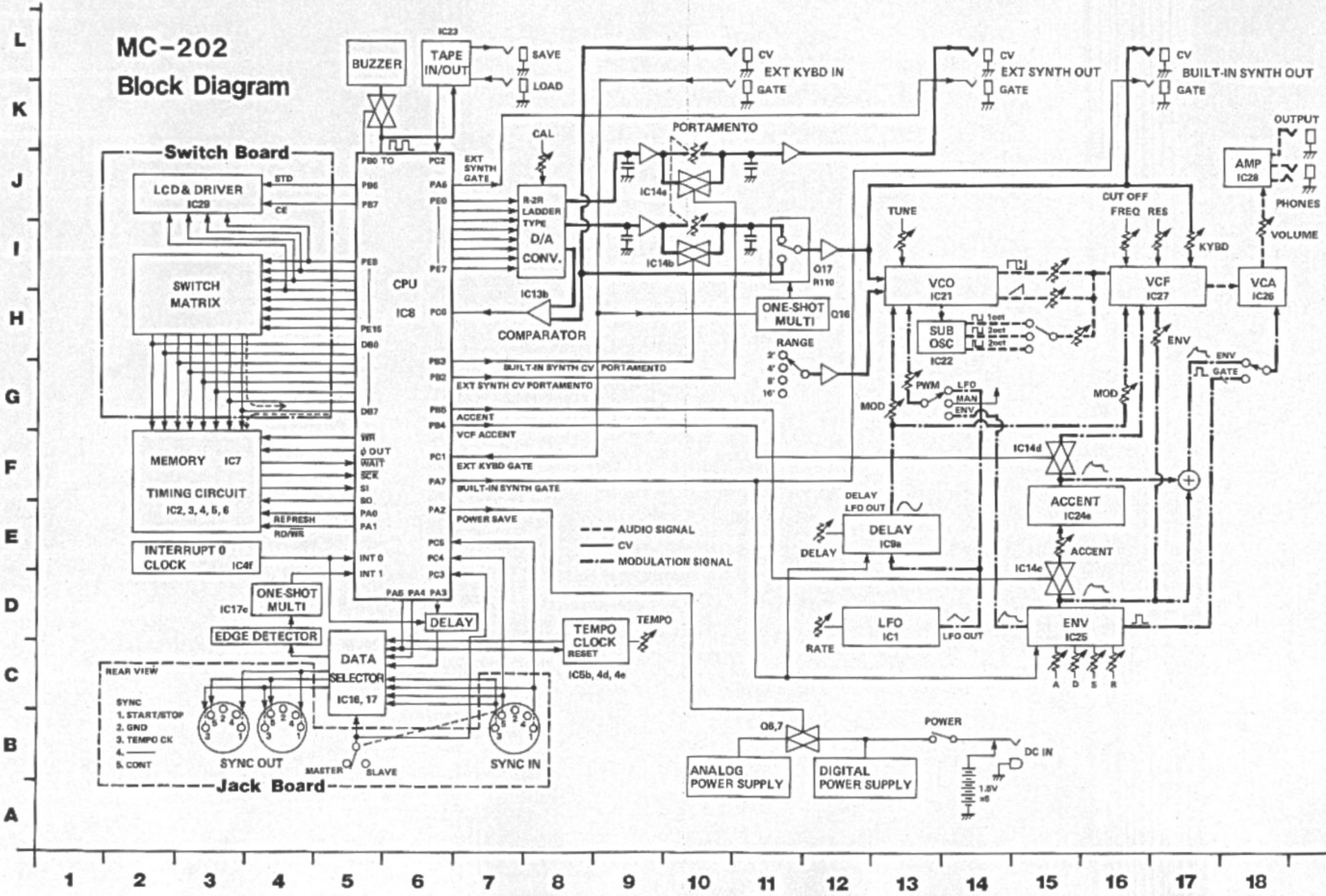
1) ADD
0.47μF across Q35(EXT CV OUT) collector and ground.
0.033μF across Q29(ENV) base and ground.

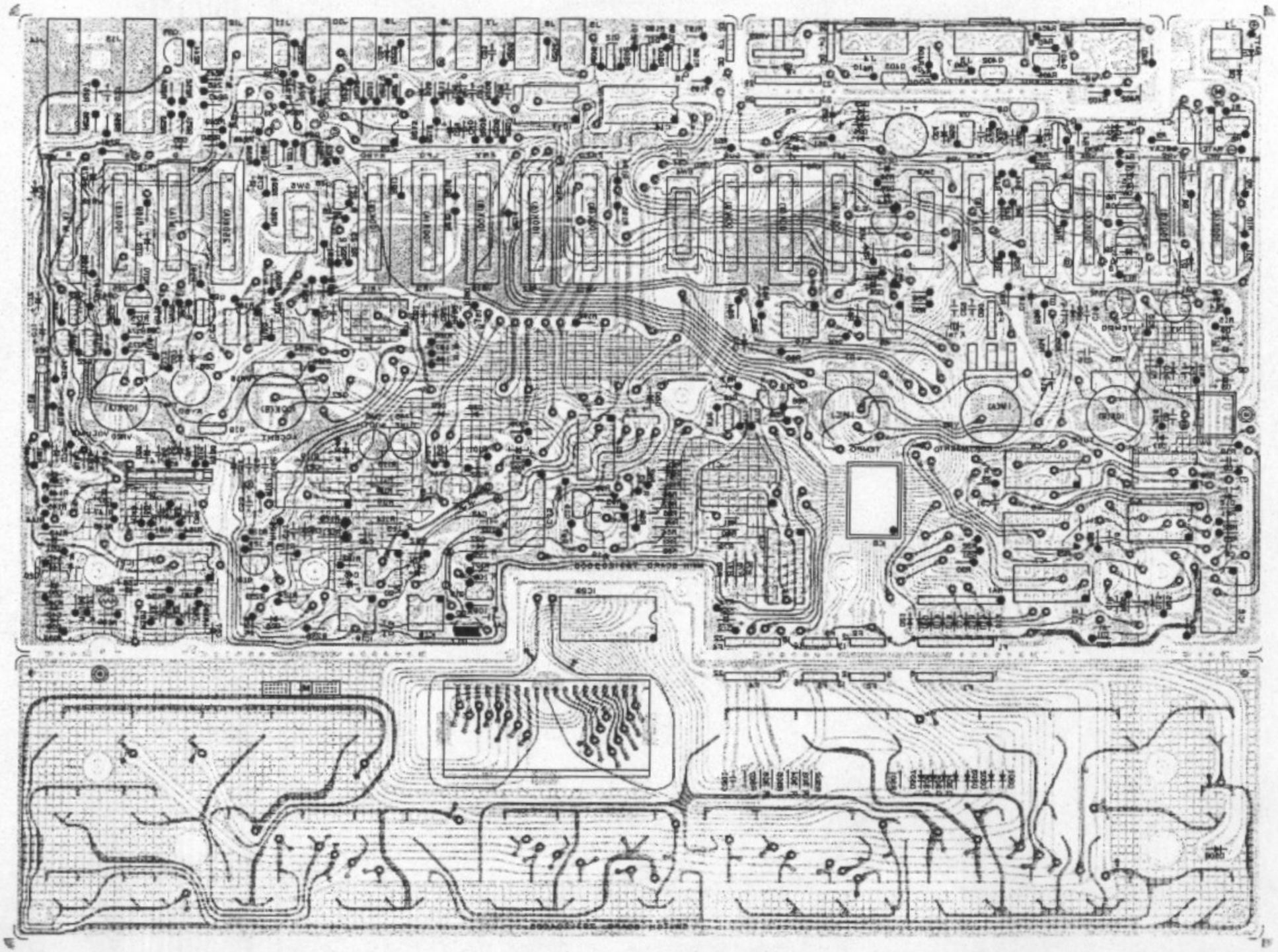
Sometimes pop or muddy sound is heard from both built-in and EXT voices when a note is followed by a new note having a great difference in frequency. This is because a new gate occurs slightly behind the CVs transition.

2) CHANGE
R56 (IC9, POWER SUPPLY) from 220 Ohms to 100.
Jumper wire between grounds of VCO and VCA.

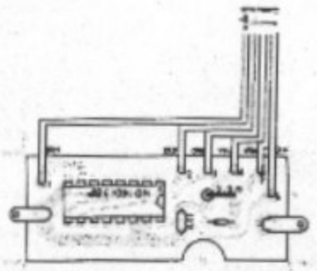
A vibrato-like effect is heard when a note around 500Hz is played with headphones jack engaged.
This is because the current returning from headphones developes a ground potential difference between the ground paths.

MC-202
Block Diagram





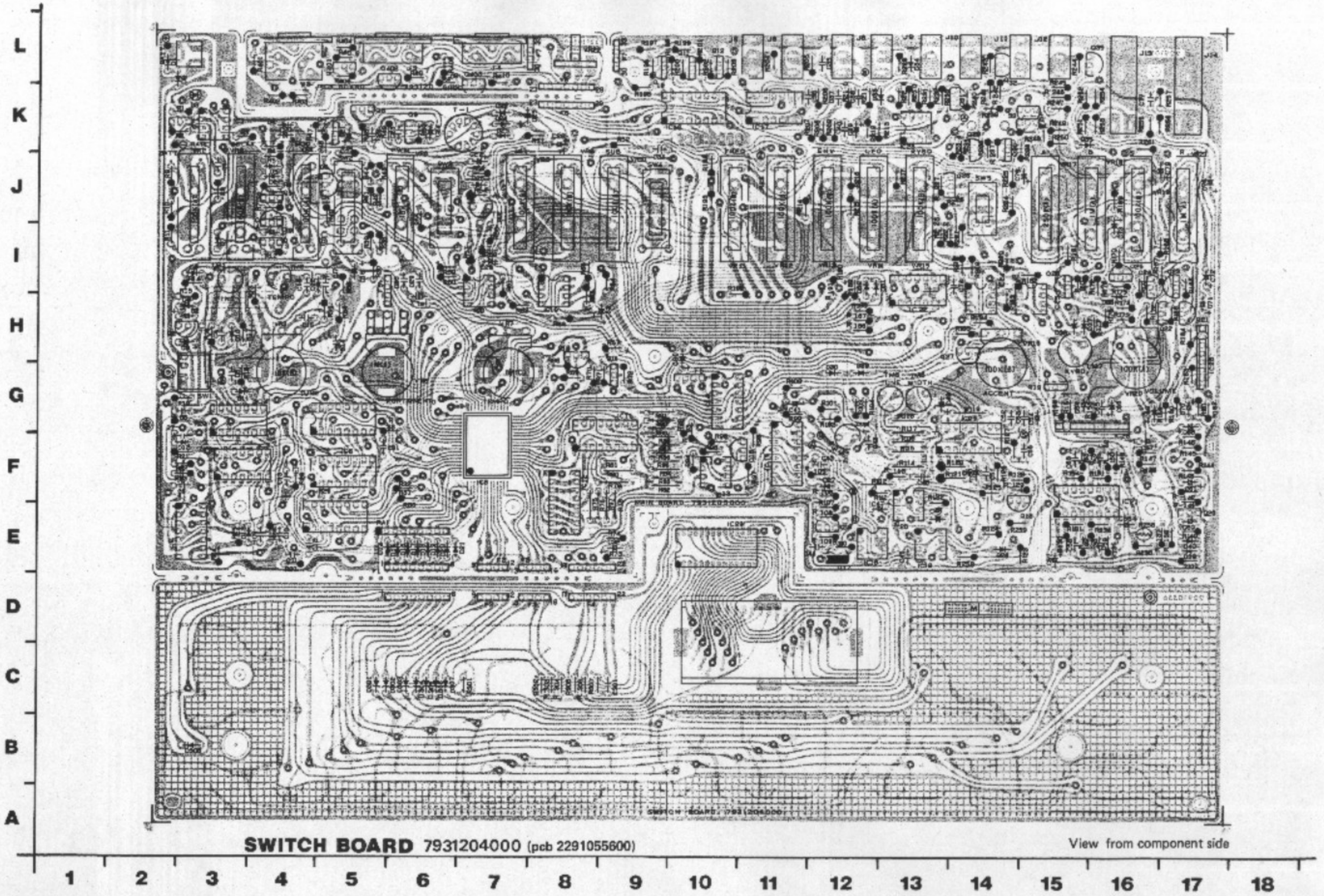
SN up to 303900
7931207000
(pcb 2291058600)



SN 304000 and up
7931207001
(pcb 2291077200)

Electrically compatible but different in dimensions.
The means of PCB support should be prepared at the location of the old PCB before replacing it with new one.

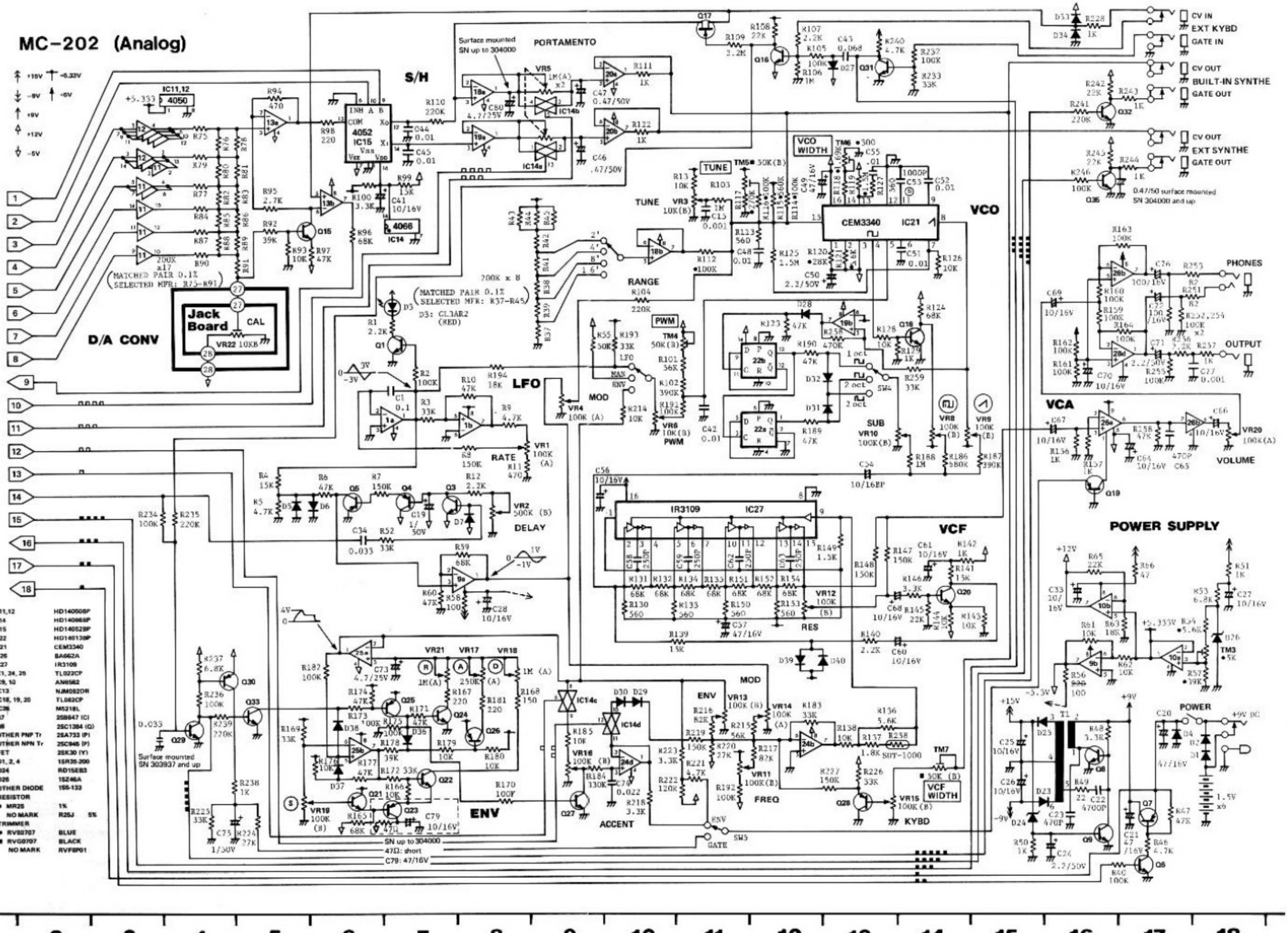
View from foil side



SWITCH BOARD 7931204000 (pcb 2291055600)

View from component side

MC-202 (Analog)



IC11,12	HD14050BP
IC14	HD14066BP
IC15	HD14052BP
IC22	HD14013BP
IC21	CEM3340
IC26	BA662A
IC27	IR3109
IC1, 24, 25	TL022CP
IC9, 10	AN6562
IC13	NJM082DR
IC18, 19, 20	TL082CP
IC28	M6218L
Q7	2SB647 (C)
Q8	2SC1384 (Q)
OTHER PNP Tr	2SA733 (P)
OTHER NPN Tr	2SC945 (P)
FET	2SK30 (Y)
D1, 2, 4	1SR35-200
D24	RD15EB3
D26	1SZ46A
OTHER DIODE	1SS-133
RESISTOR	
● MR25	1%
NO MARK	R25J 5%
TRIMMER	
● RV60707	BLUE
■ RVG0707	BLACK
NO MARK	RVF8P01

CIRCUIT DIAGRAM (Digital)

MC-202 (Digital)

IC2	HD14001BP
IC3	HD14011BP
IC4	HD14584BP
IC5	HD14520BP
IC6	HD14503BP
IC7	MSK4164P-20
IC16	HD14519BP
IC23	TL022CP
IC29	MN12528
Q2	2SD667 (C)
OTHER NPN Tr	2SC945 (P)
All PNP Tr	2SA733 (P)
D9	RD5.6JB2
OTHER DIODE	1SS-133
RESISTOR	R25J 5%
POT	RVF8P01

IC7 64 K bit D-RAM ADDRESS

IC5a 1/2 4520

IC5b 1/2 4520

IC8 CPU μPD78C06G-024

IC29 MN 12528

IC30 4015

IC16 4519

RNSA-09P473 47K x 8

EDD063M0483

Switch Board

Jack Board

Delay Board

Delay Board

Switch Board

SURFACE MOUNTED

SYNC
1. START/STOP
2. GND
3. TEMPO CLOCK
4. ——
5. CONT.

SYNC IN SYNC OUT 1 SYNC OUT 2

Fig. A

SN30400-up MOUNTED ON Delay Board

PIEZO ALARM PKM24-4A0

SAVE LOAD

METRONOME ON/OFF

TAPE IN

S/H SELECT

=BUILT-IN SYNTH =EXT SYNTH

MSB D/A LSB

A/D COMPARATOR OUT

EXT SYNTH CV PORTAMENTO ON/OFF

BUILT-IN SYNTH CV PORTAMENTO ON/OFF

VCF ACCENT ON/OFF

ACCENT ON/OFF

BUILT-IN SYNTH GATE ON/OFF

EXT SYNTH GATE ON/OFF

EXT KYBD GATE IN ON/OFF

POWER SAVE ON/OFF

MASTER/SLAVE

CONT

START/STOP

BATTERY CHECK LIVE/DEAD

TEMPO

CONT

S/S

LCD DRIVE

REF/ACCESS

RD/WR

WR

WAIT

RESET

INT 0

INT 1

TEMPO

CONT

START/STOP